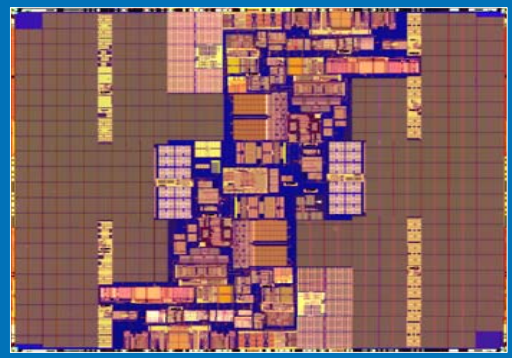
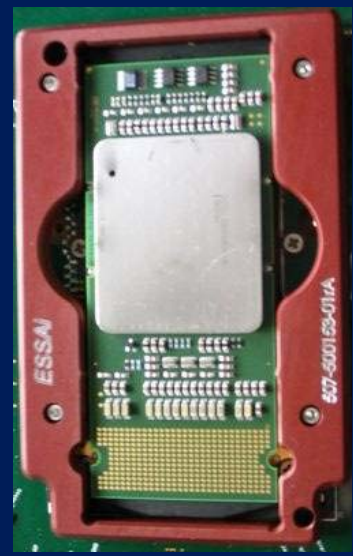




Montecito, an inside look at the new generation

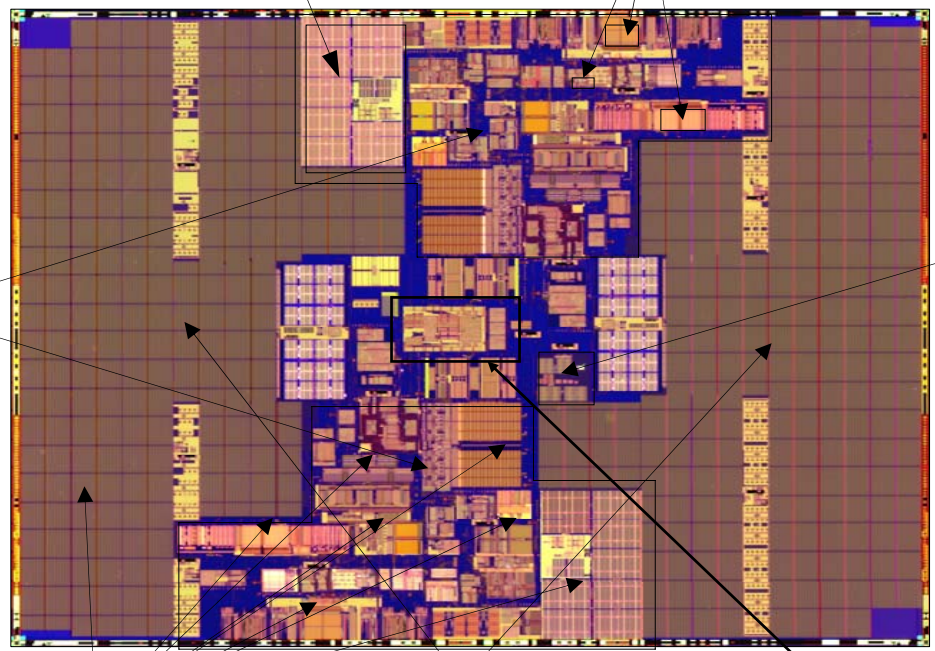
Dr. Ingolf Buttig
Technology Consultant
Hewlett-Packard GmbH

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The information contained herein is subject to change without notice

Agenda

- **Montecito Overview**
 - Exploiting parallelism at all levels
 - Instruction Level Parallelism
 - Thread Level Parallelism
 - Foxton technology- Dynamic power management
 - Pellston technology - RAS and manageability
 - Silverdale technology - Intel hardware virtualization
- Performances – *estimated* -
- Operating system design implications
 - HP-UX
 - OpenVMS
 - Windows
 - Linux

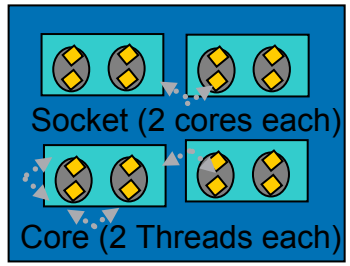
Introducing Montecito





Montecito overview

- Multi-threading
 - 2 cores / socket or cpu; 2 threads / core
 - Processor core and memory hierarchy is based on Itanium® 2
 - With improvements in control, data paths and resources
 - McKinley bus compatible
 - CMT /SOEMT (Switch- On- Event) Multi-threading
 - Switches occur on event (on cache misses, hints, timeout, …)



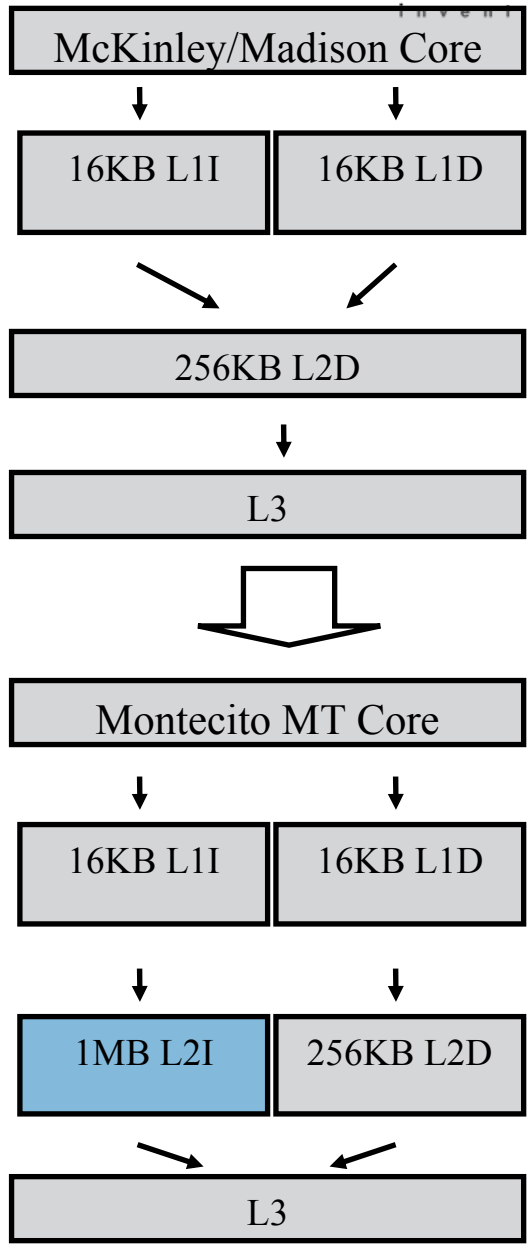
- Pellston
 - Mapping out (disabling) of cache lines with errors to avoid hard errors that would crash the partition
- Foxton
 - Dynamically adjust the frequency to maintain a chosen power state, all based on workload (called activity factor)
 - Montecito also supports more than one power state (P-state)
- Silverdale
 - First IPF processor to implement Virtual Machine hooks to ease the implementation of VM monitors (Vanderpool/VT on x86)

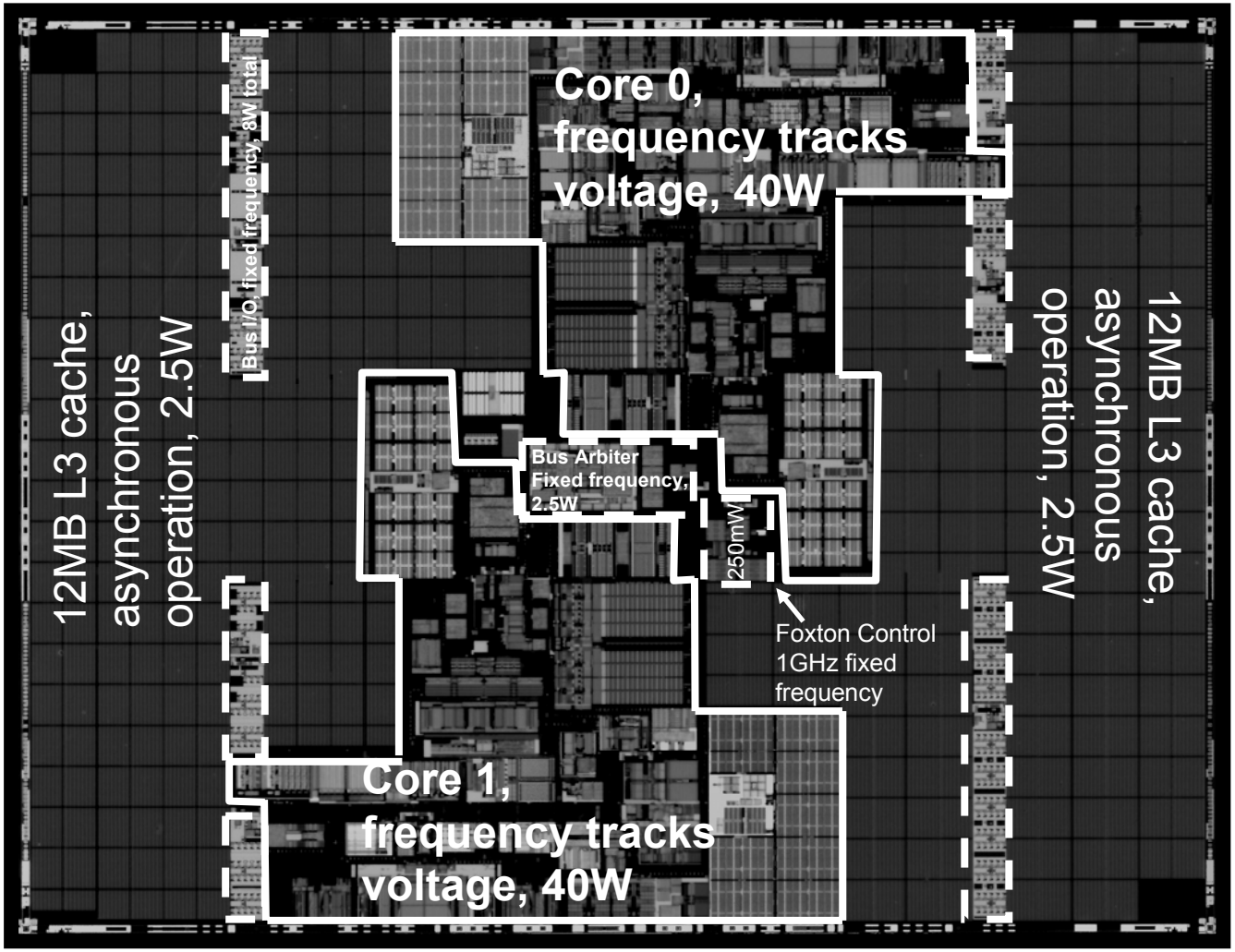
Montecito overview

- Technology
 - 2.0/2.2 GHz core speed
 - 100 W
 - 90 nm
- Cache (26.5MB total)
 - Maximum 12 MB L3 cache per core (24MB total, non-shared)
 - Maximum L3 associativity 12
 - Minimum L3 access time of 14 cycles
 - The L2 cache has been split into separate L2I (1MB) and L2D (256KB) caches per core
 - 16 KB L1I, 16KB L1D per core
- RAS + Manageability features
 - Additional ECC and parity for structures
 - ECC add in L2T tags, and parity added to L1I TLB
- First die with over 1 billion transistors (1.72B total)

Core design changes

- CMT/SOEMT Multi-threading
 - Very low cost throughput performance boost
- New level of cache – 6 cycle 1MB L2I
 - Addresses largest component for transaction processing (Instruction misses)
 - Frees 256KB L2D to be dedicated for data
- Second shift/merge unit for encryption performance
- Power reduction with support for dynamic frequency and voltage



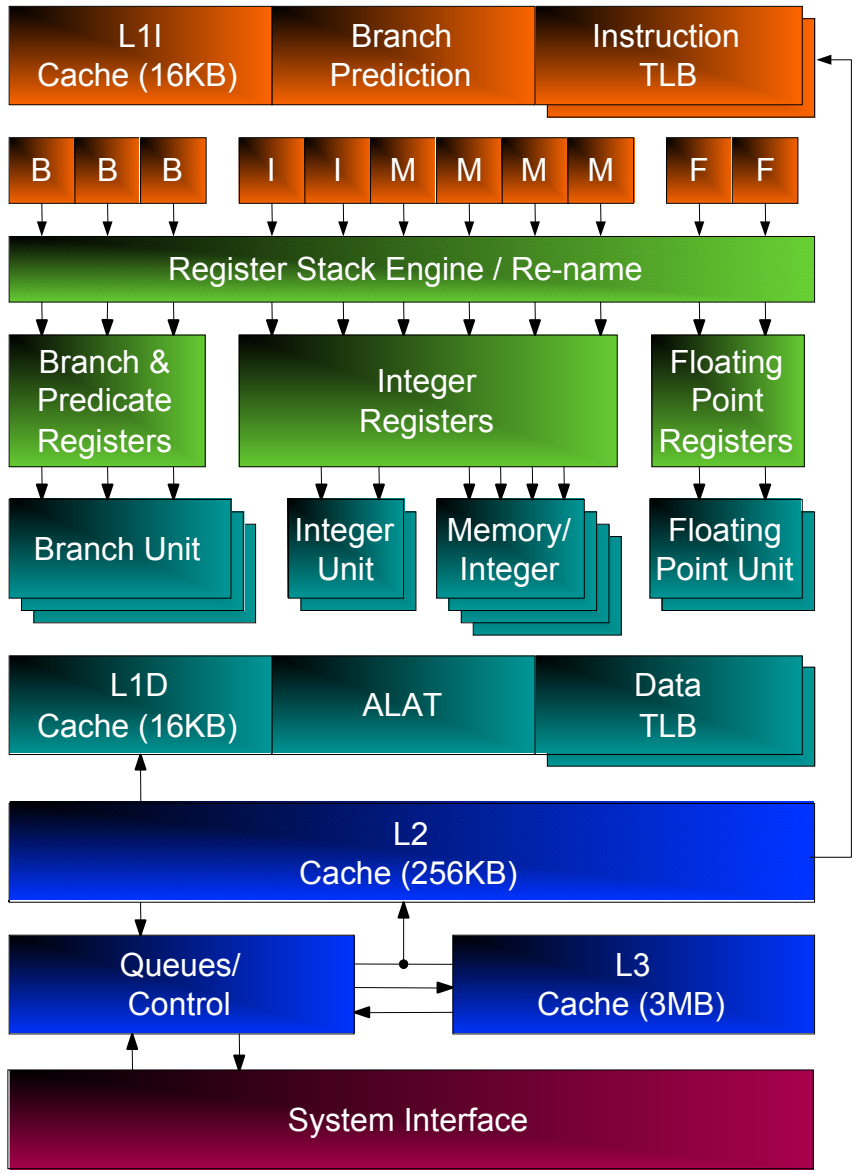


Chip power consumption

Domain	Voltage	Frequency	Power
Cores	.8 – 1.2V	Tracks voltage	80W total
Cache	.9-1V	Self-timed	5W total
IO term	1.2V	Bus	8W total
Fixed	1.15V	Fixed	6W total

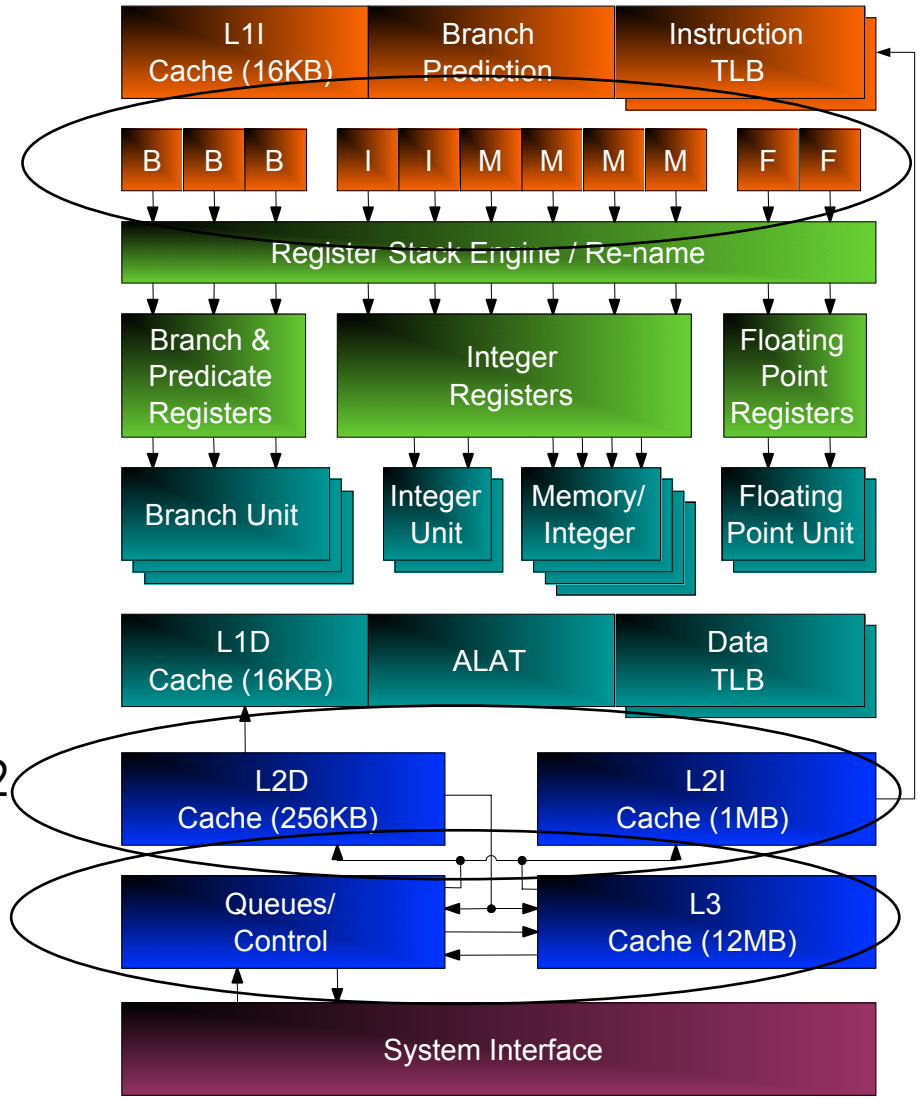
Building on Itanium® 2

- Compatibility
 - Same capable micro-architecture supports familiar optimizations
 - Same system interface allows for leveraged investment
- Performance
 - Continue and expand Itanium® 2 performance trends
 - Introduce new performance opportunities
- Efficiency
 - 2 cores, 2 threads, 26.5MByte of cache, and 1.72 billion transistors at 100W
- Flexibility
 - Dynamic power and frequency management
 - RAS+M



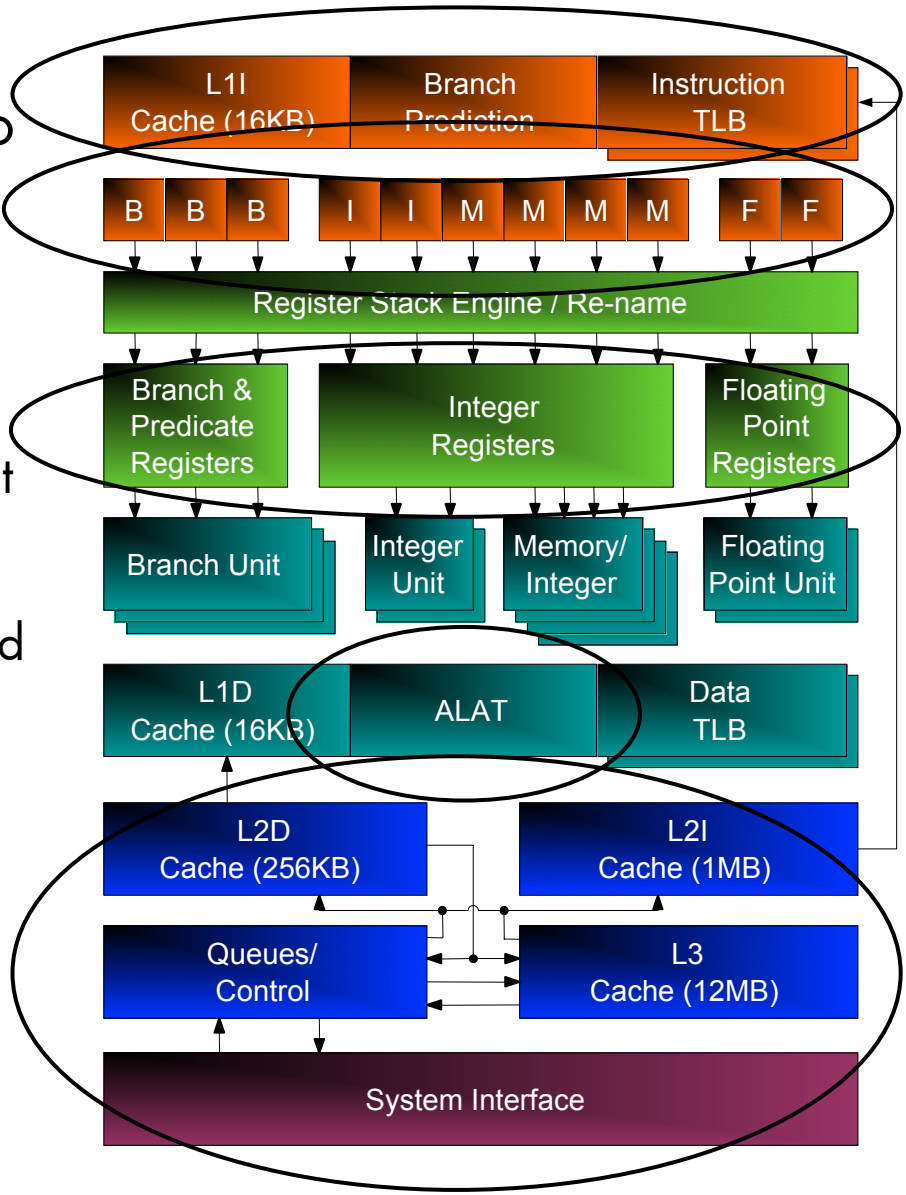
Improving ILP

- Improving execution
 - New instructions
 - Additional functional units
 - More efficient speculation recovery
- Improving the memory hierarchy
 - Split the L2 cache
 - Dedicated 1 MByte L2 instruction cache
 - Reduced pressure on L2 data cache
 - Larger L3
 - Grown L3 to 12 MByte
 - Maintain L3 latency of Itanium® 2 processor 6M and 9M
 - Queues and Control
 - Additional L3 and L2 victim buffers
 - More efficient control of queues and coherence

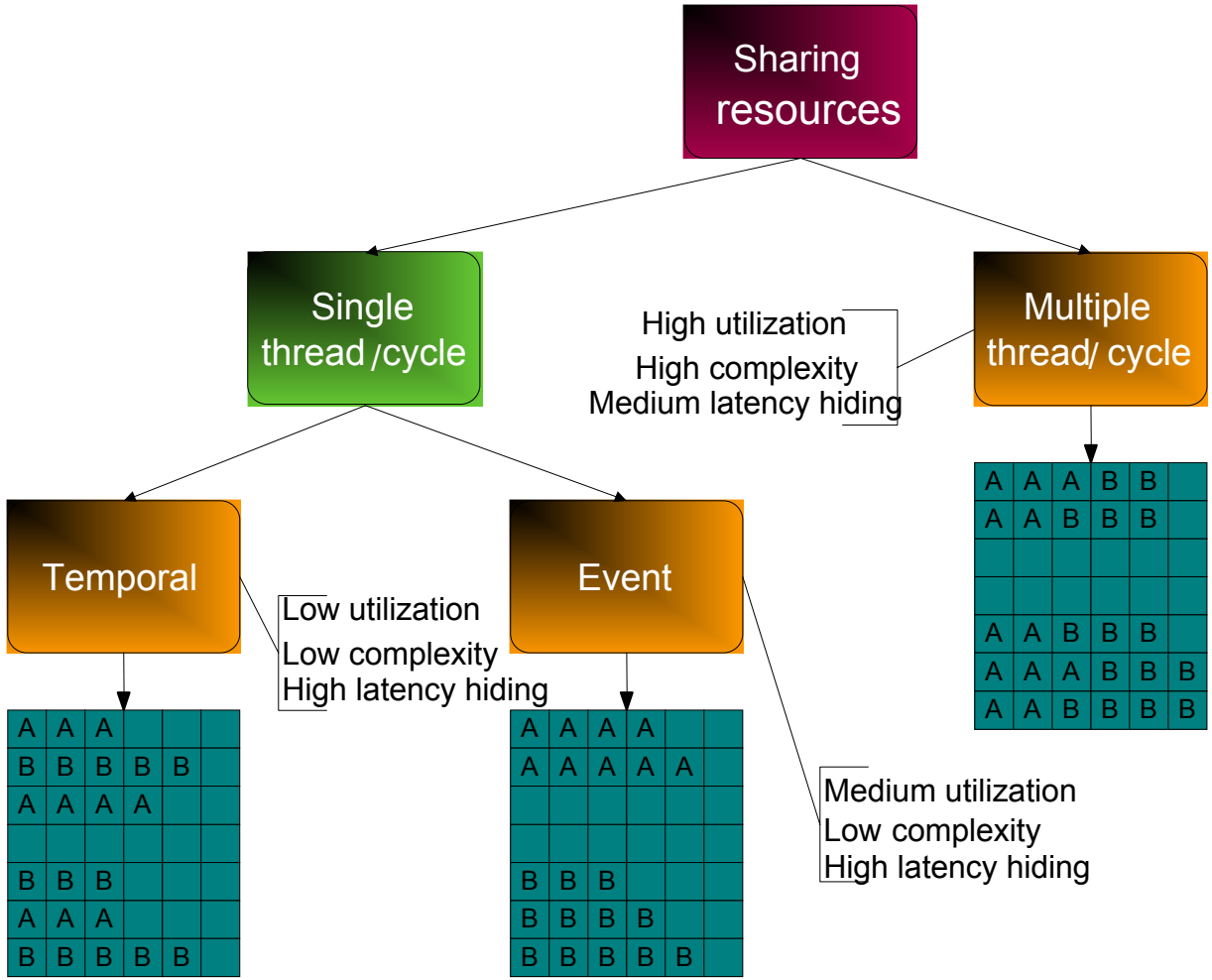


Exploiting TLP

- Interleave independent threads to hide memory latency
 - Multiple cores in each socket
 - Multiple threads in each core
- Montecito multi-threading
 - Maintains 1 set of execution units but 2 sets of architectural state to switch quickly between threads
 - Dynamically allocate resources based on most efficient use
 - Long latency events or completion determine if a thread can effectively use execution resources
- Execution Resources
 - Shared
 - Competitively/Symmetrically
 - Temporally
 - Dedicated/Partitioned

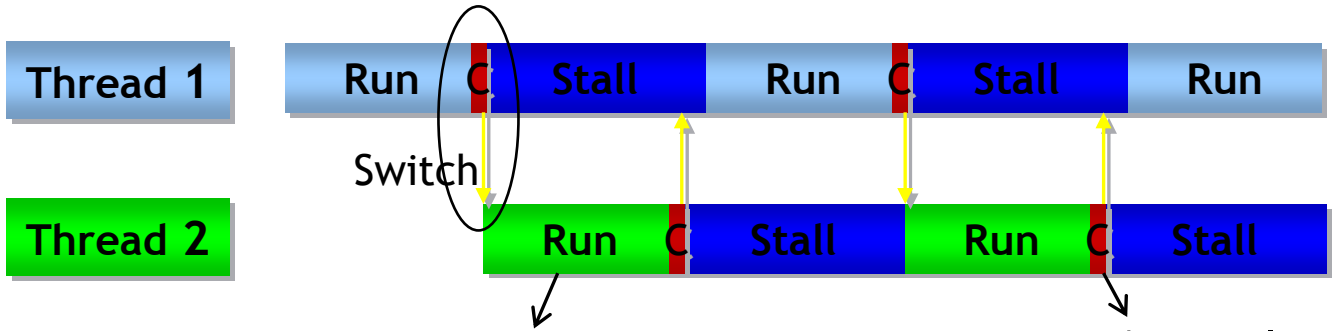


Multi-Threading approaches



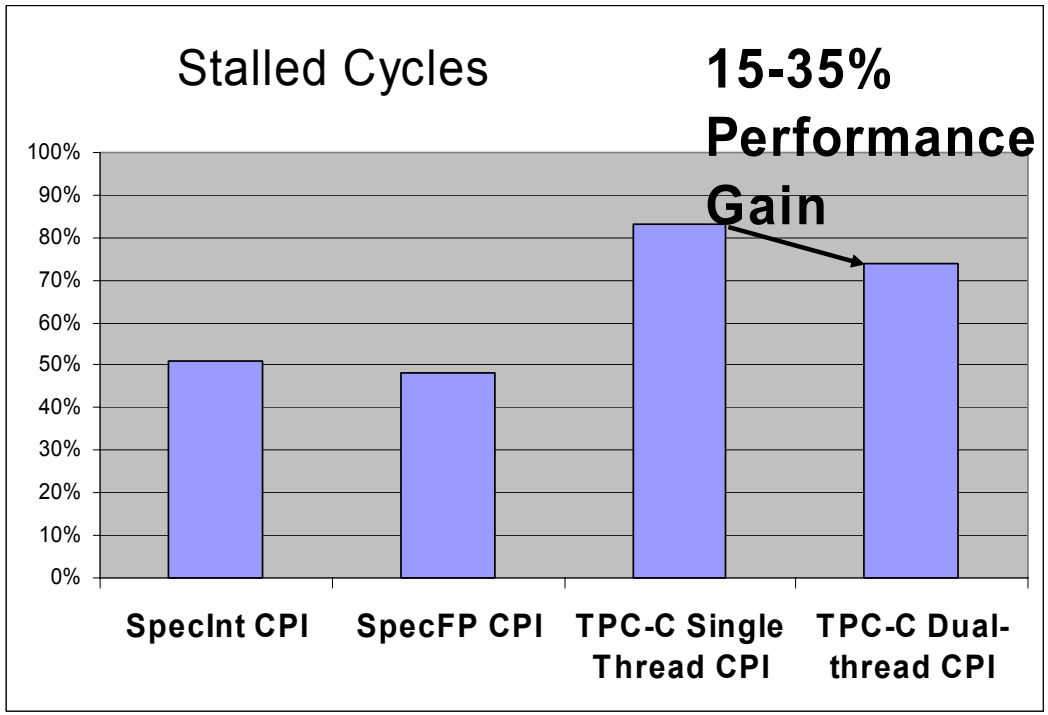
Multi-threading decreases stalls and increases performance

Montecito Multi-Threading Execution



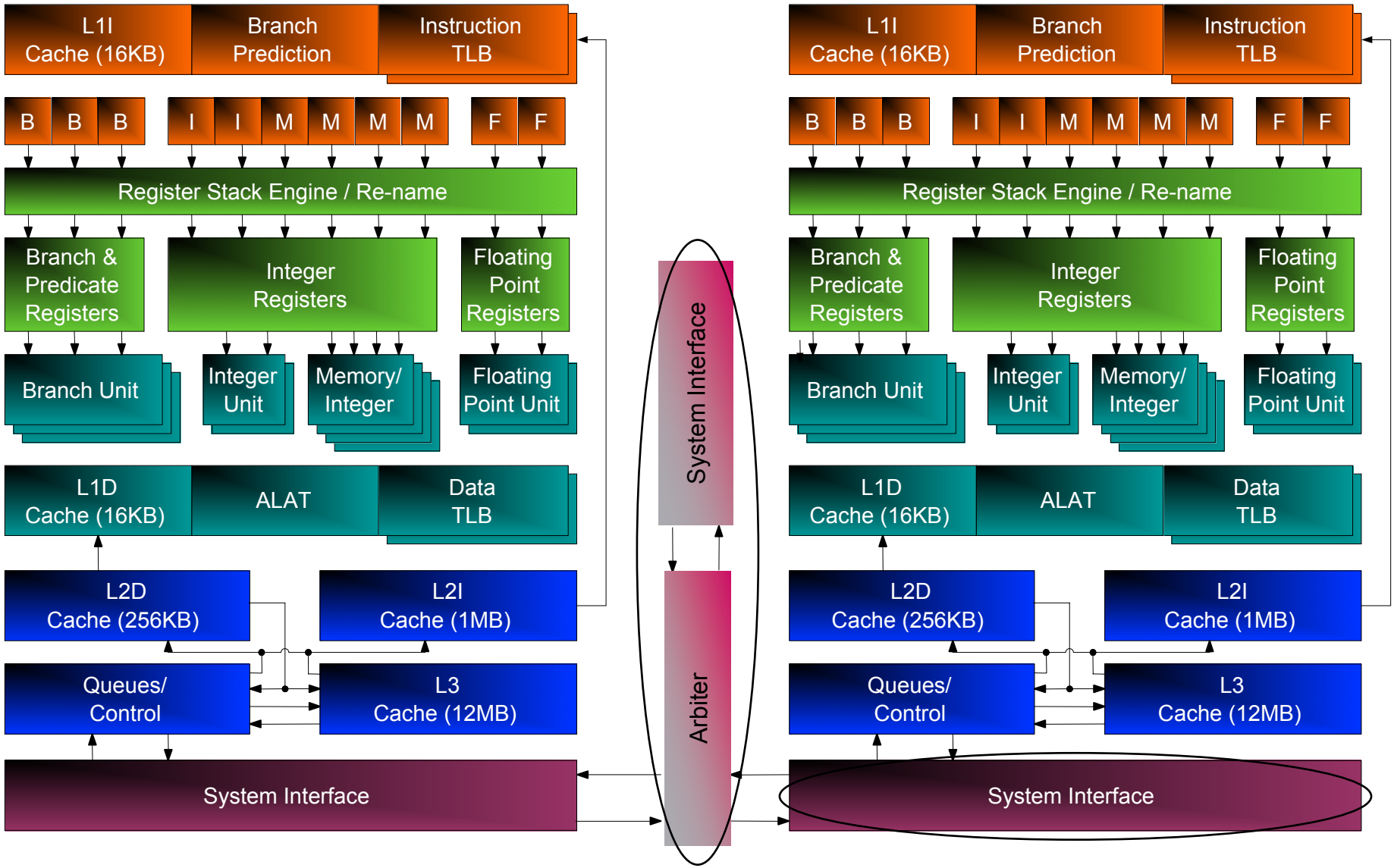
Overlap memory latency stall of Thread 1 with execution of Thread 2

15 cycle penalty



2% core area impact

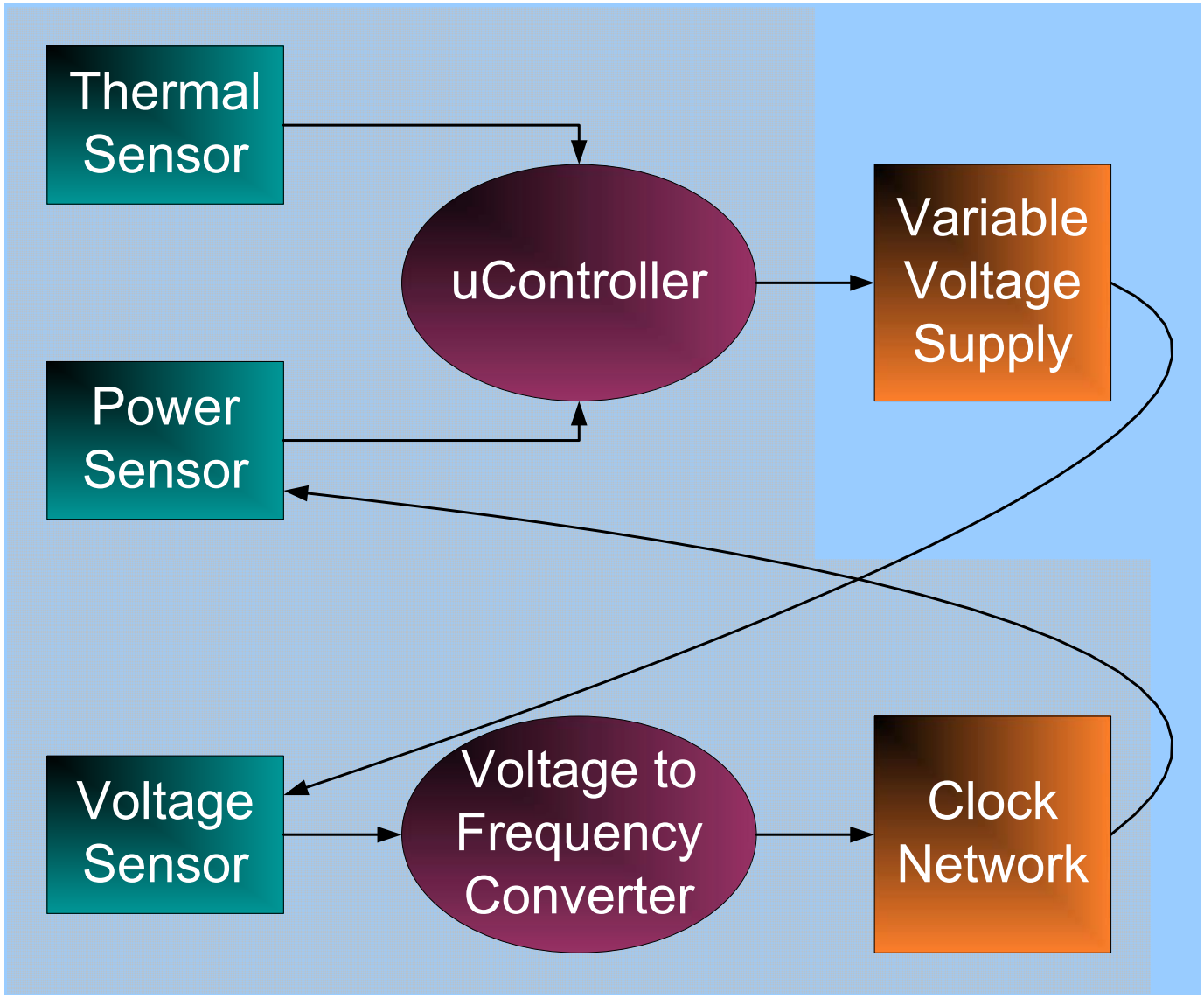
Dual Cores


L1I Cache (16KB)
Branch Prediction
Instruction TLB
B B B
I I M M M M
F F
Register Stack Engine / Re-name
Branch & Predicate Registers
Integer Registers
Floating Point Registers
Branch Unit
Integer Unit
Memory/ Integer
Floating Point Unit
L1D Cache (16KB)
ALAT
Data TLB
L2D Cache (256KB)
L2I Cache (1MB)
Queues/ Control
L3 Cache (12MB)
System Interface
System Interface
Arbiter
L1I Cache (16KB)
Branch Prediction
Instruction TLB
B B B
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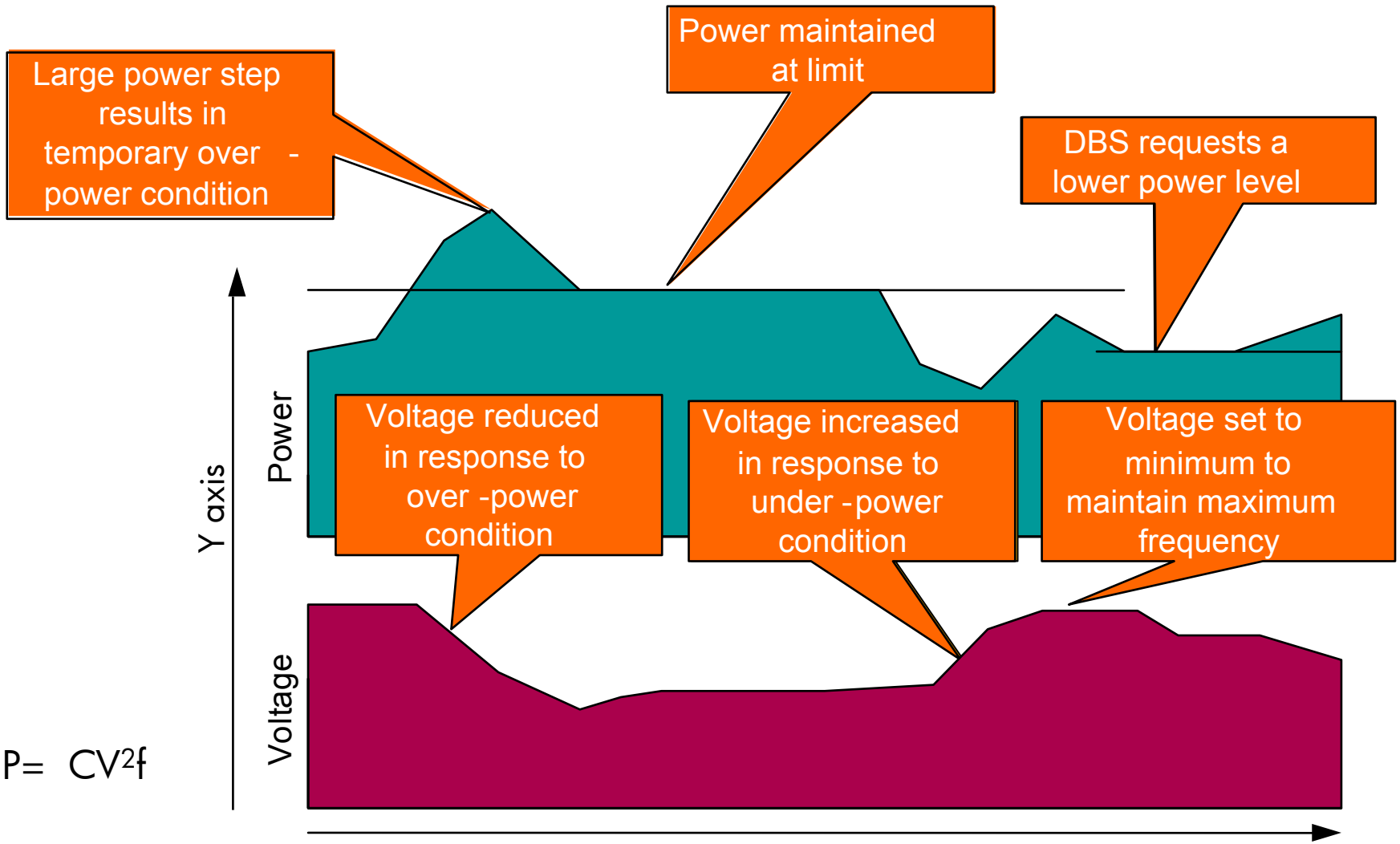
Foxton Technology

- Dynamically adjusting Voltage (V) and frequency (f) allowing applications to exploit full power envelope
 - Monitor/calculate power and temperature
 - Set Voltage to the minimum value needed to support highest frequency
 - Over power and/or temperature results in voltage change
 - Frequency responds to global and local voltage
 - Large power change → small voltage change from **$P=CV^2f$** (C=Capacitance of the gate)
 - 3% power change with only 1% voltage change
 - Optimized around a TPC-C activity factor
 - Activity factors (AF) – the switching power an application is likely to experience -- $P= AF * CV^2f$
 - Enterprise < Integer < Technical < Any known application
- Supports Demand Based Switching and OEM selectable power envelopes

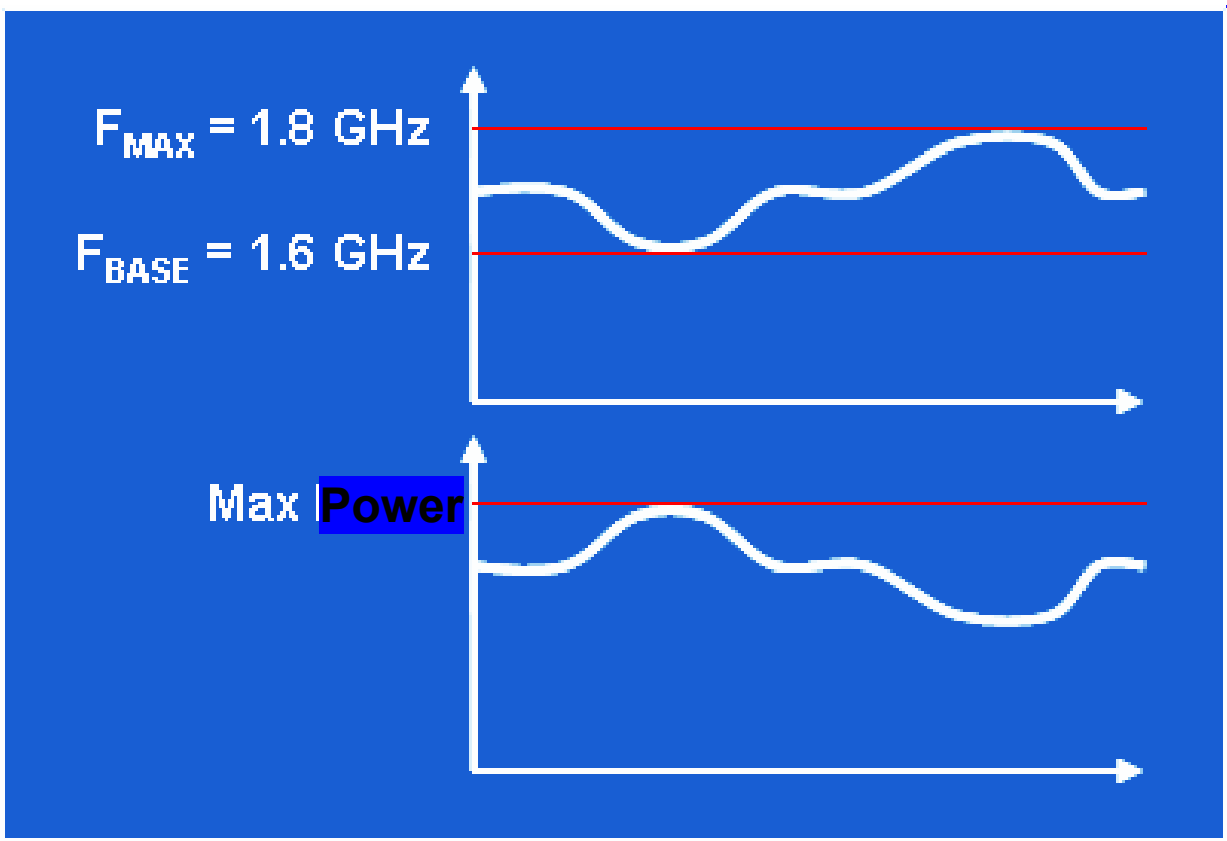
Foxton Technology



Foxton Technology
Power and Voltage Interaction

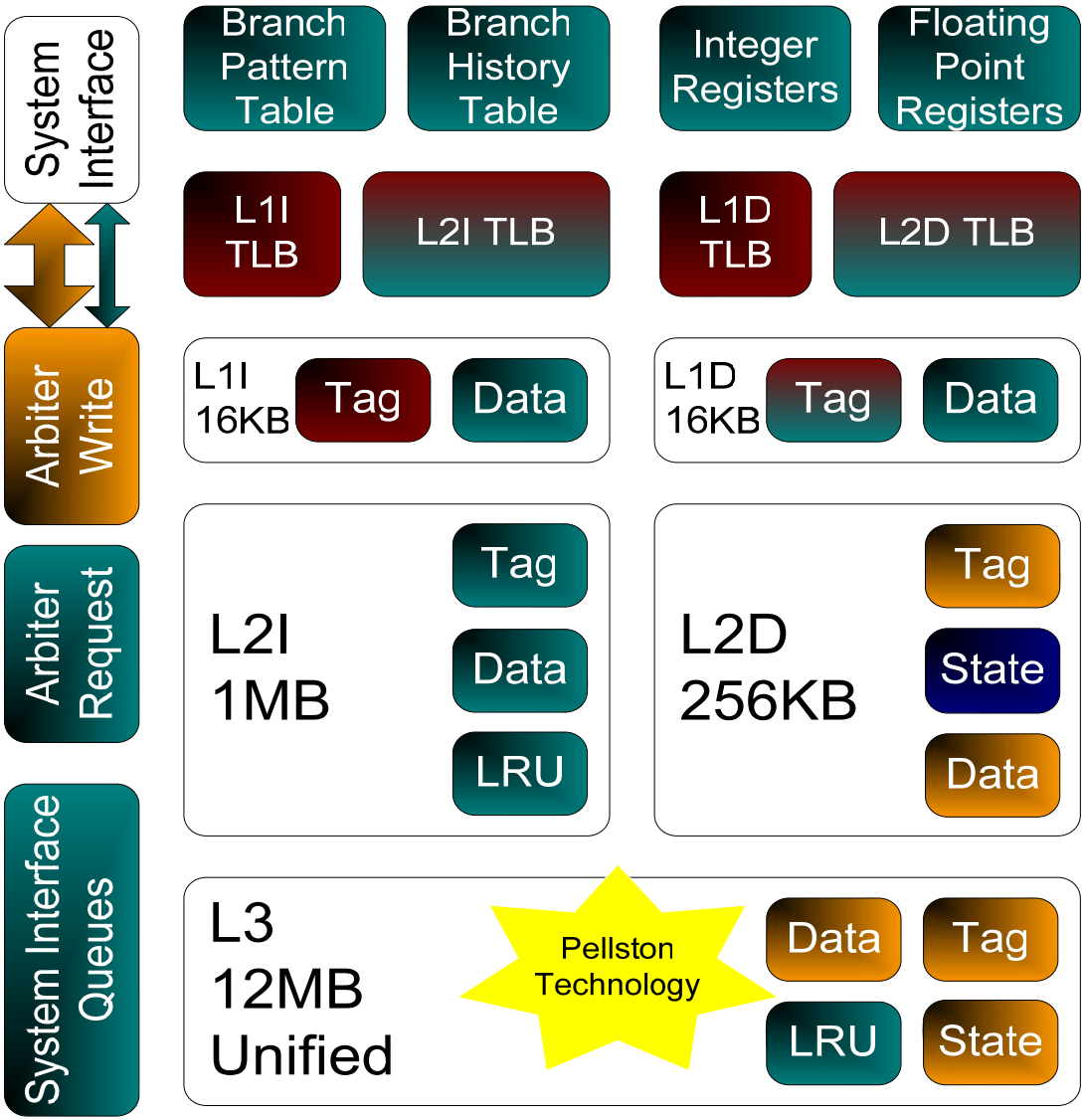


Foxton Technology adjusts processor frequency within power



Foxton provides headroom to increase clock speed and achieve performance gains!

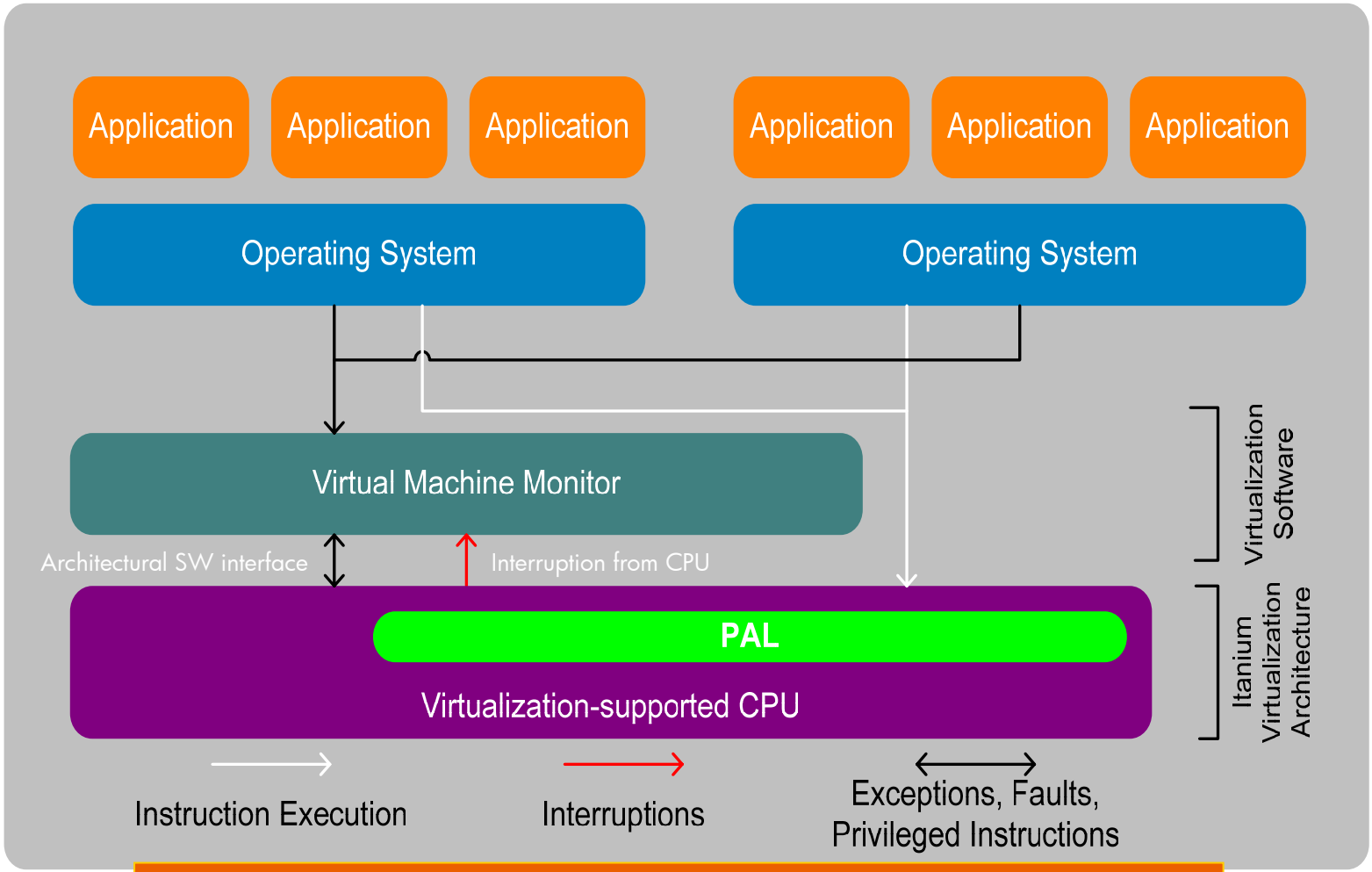
Pellston Technology, Error Protection



- Protection is adapted to the structure
- Pellston identifies and correct transient errors in cache lines and shuts down faulty cache lines
- Pellston improves reliability

ECC
Parity
Multiple Hit
1 From Modified

Silverdale (VT-i) Technology Virtualization



Multiple guest OSes on a single processor

Intel Virtualization Technology

Intel Virtualization Technology (VT-i) improves the reliability security and supportability of virtualization SW solutions

- Key features:
 - A new, higher privilege ring for the VMM
 - Hardware-Based Transition
 - Handoffs between the VMM and guest OSs are supported in hardware
 - Hardware-Based Memory Protection
 - Processor state information is retained for the VMM and for each guest OS in dedicated address spaces
- Key advantages:
 - No need for binary translation
 - Eliminate performance overhead of SW virtualization
 - Simplify VMM development and maintenance
 - Allows VMMs to be written to common standard and to be more robust

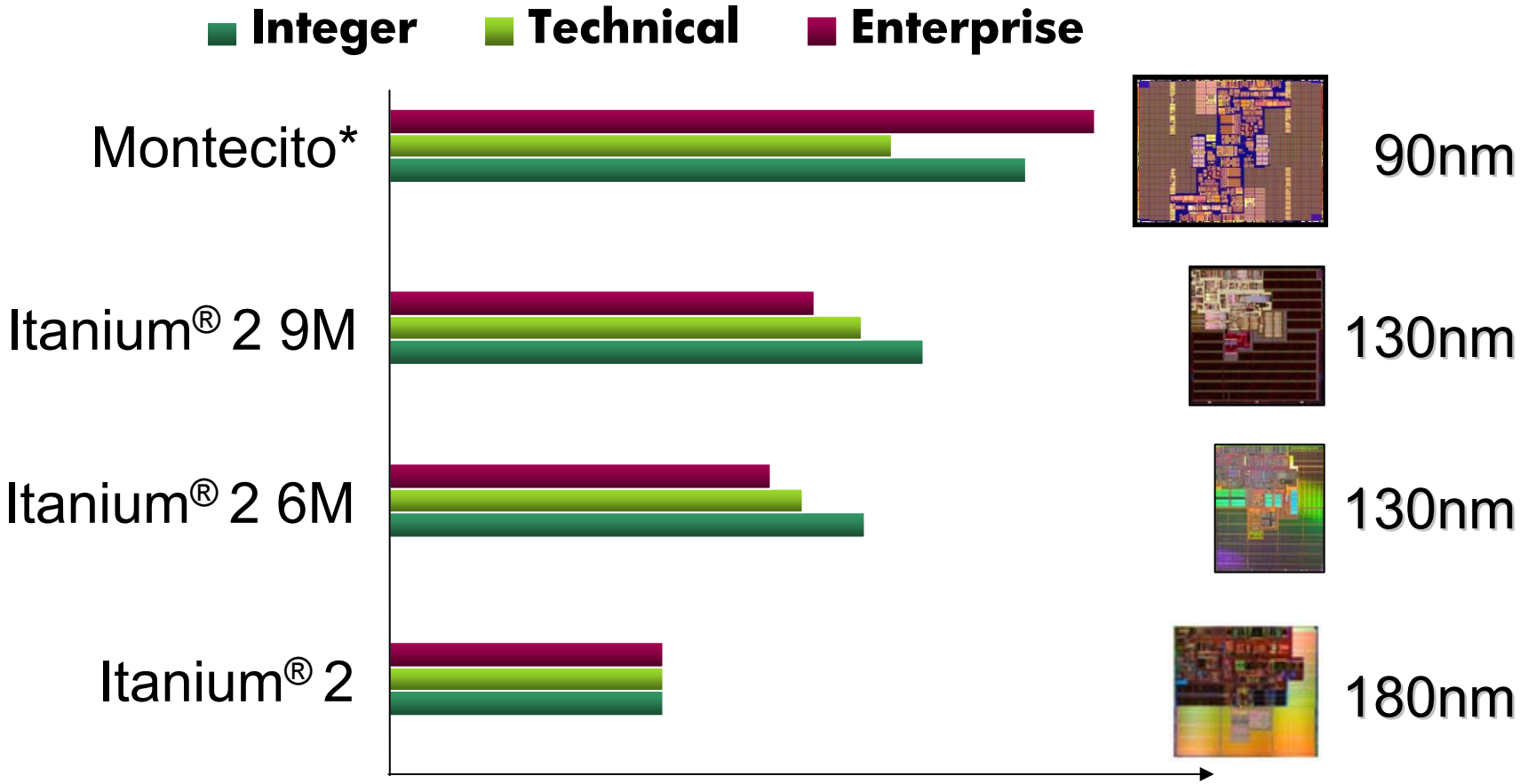
Performance Monitor

Feature	Itanium®2	Montecito
Event Counter Regs	4	12 (per trd)
Branch Trace Buffer	8	16 (per trd)
Lev 2 Cache	restricted	Less restricted
Opcode filtering	partial	Full 41 bits
IP trace capture	No	yes
New events		L2 I-cache, L3 state, Multi Threading, Foxton, Arbiter

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 - OpenVMS
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 - Linux

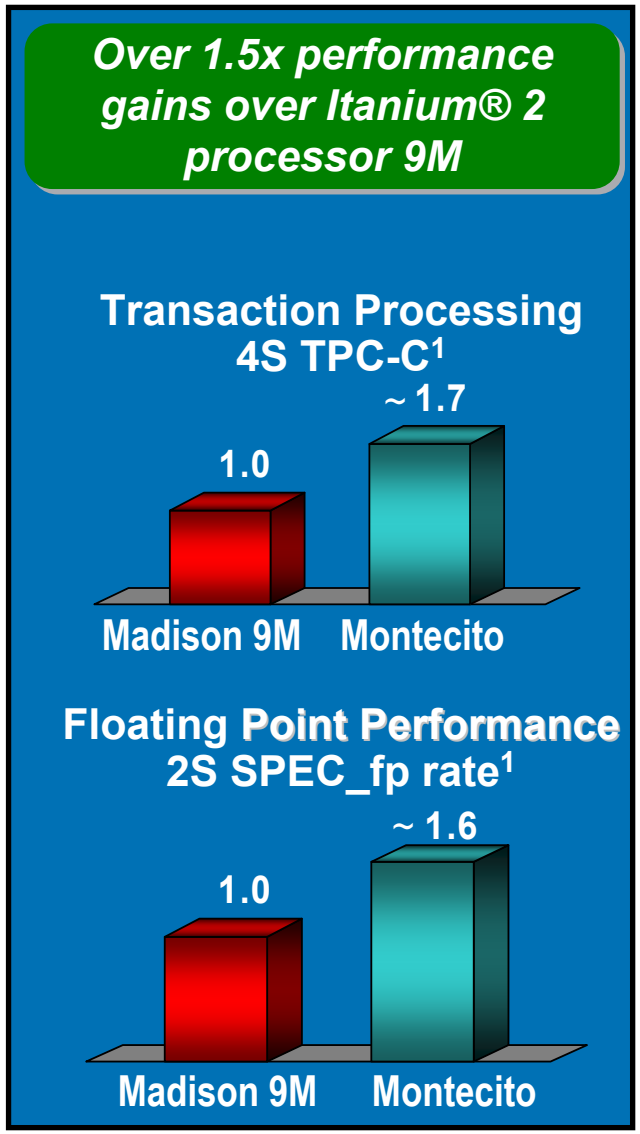
Itanium® 2 Performance



Performance with multiple cores, multiple threads, larger caches, and higher frequency

Technologies influence on performances

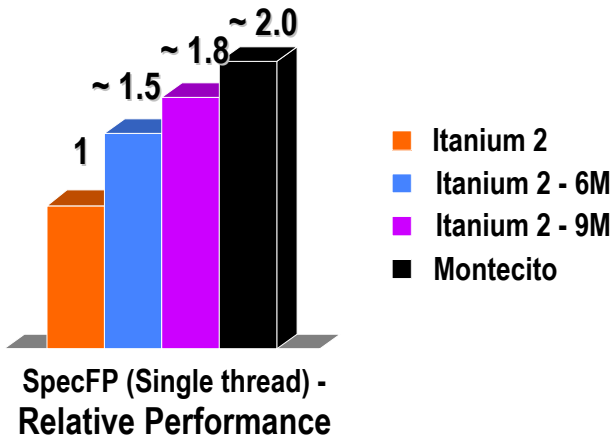
- **Dual core:** more performance and throughput
- **1.5 – 2X the performance:** plus Foxton Technology to dynamically boost performance
- **2.5X the cache:** Up to 24MB on-die L3 cache
- **4X the threads:** MT - 4 threads/socket
- **Enhancement to premier reliability:** Pellston Technology improves system reliability and availability
- **Robust virtualization:** Silvervale Technology, more robust reliability, flexibility, efficiency and security
- **Lower power:** Demand Based Switching reduces power consumption dynamically based on CPU utilization



Performance Innovations

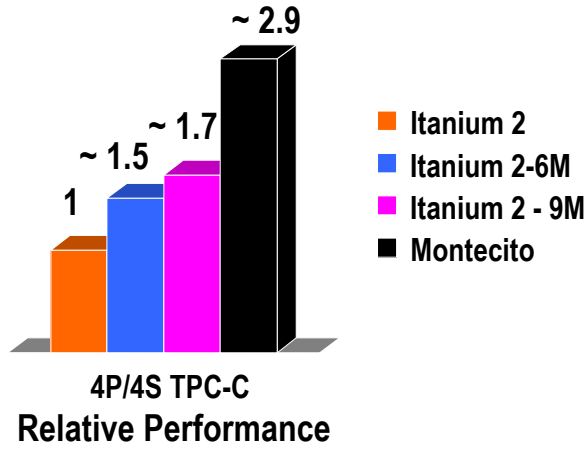
- Itanium® Performance Strategy: Increased performance/thread, then increased number of threads

Increased Performance/Thread



- Driven by:
 - Increased frequency
 - Increased L3 cache
 - Increased bus speed

Performance From Threads



- Driven by:
 - Dual core Montecito
 - Multithreading support in Montecito

Sources:
Itanium 2 to Itanium 2-6M: www.spec.org and www.tpc.org
Itanium 2-9M and Montecito: Intel estimates.

Itanium® Innovation driving performance beyond Moore's law

Linkpack peak, 4 cpu server

McKinley	Madison 6M	Montecito	p5
1 GHz	1.5 GHz	1.6 GHz	1.9 GHz
16 gflops	32 gflops	**64 gflops**	60 gflops

Chip for chip and core for core, a slower Montecito seems to be beating a faster Power5 on the Linpack test!

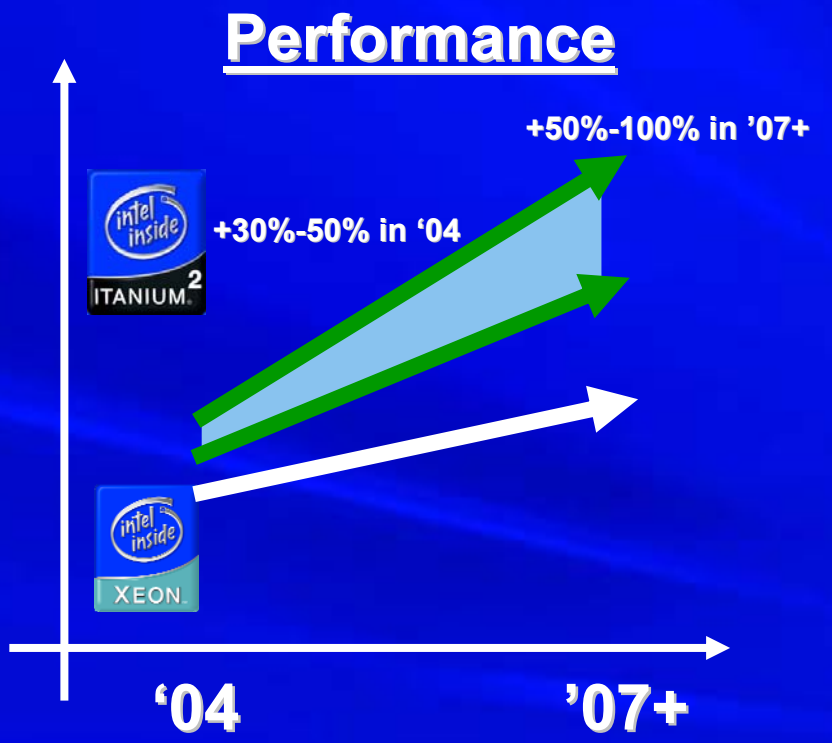
Next leap frog P5+ vs. Montecito 2.0Ghz ☺

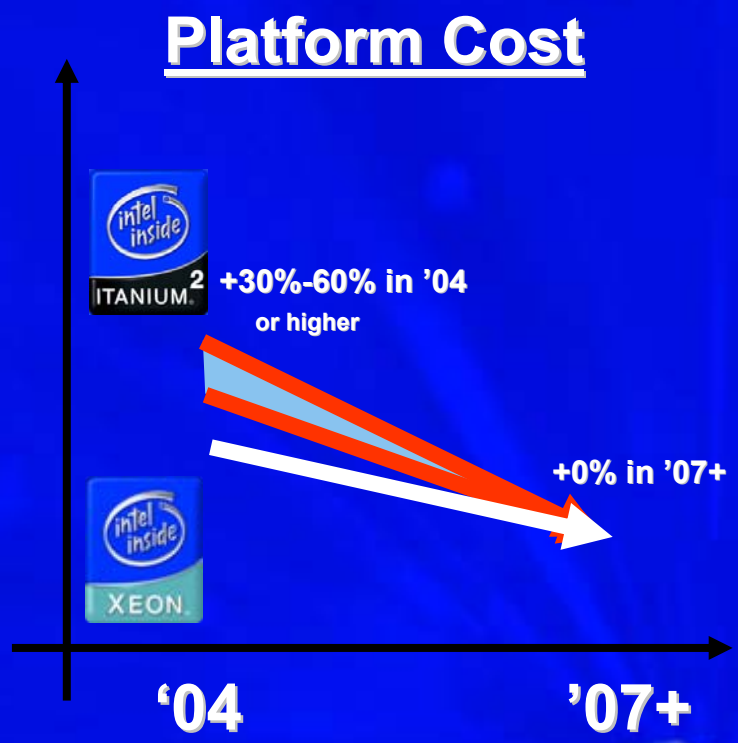
Itanium® Processor Plans

All products, dates and information are preliminary and subject to change without notice.

On track to deliver 1.5-2X better performance than Xeon processor

…plus cost parity with Xeon processor based platforms
(via common platform infrastructure)





Source : www.ioncomputers.com, www.dell.com
ION SR4004, (4) Xeon processors 2.8 GHz, 2MB cache, 24 GB system memory, 36 GB HDD, no OS - $34,616
ION I2X4, (4) Itanium 2 processors 1.5 GHz, 6 MB cache, 24 GB system memory, 36 GB HDD, no OS - $44, 950
Dell PowerEdge 2650, (2) Xeon processors 3.2 GHz, 1 MB cache, 4 GB system memory, 36 GB HDD, no OS - $6,143
Dell PowerEdge 3250, (2) Itanium 2 processors 1.4 GHz, 1.5 MB cache, 4 GB system memory, 36 GB HDD, no OS - $9,499

* Other names and brands may be claimed as the property of others.

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- **Operating system design implications**
 - HP-UX
 - OpenVMS
 - Windows
 - Linux

HP-UX and Montecito technologies

- Multi-threading
 - Yes
- Pellston
 - Yes , not OS dependent
- Foxton
 - Yes
- Silverdale
 - Post announcement HP-VM version

HP-UX and Multi-threading

- Utilization of the hardware threads in Montecito requires HP-UX 11i version 2 December 2005 at a minimum
- The threading of Montecito is transparent to software applications; no special programming is necessary to take advantage of Montecito threading
- Specifically, applications certified on earlier Itanium® processors will run unmodified on Montecito;

 No re-programming or recompilation is necessary to take advantage of Montecito threading
- Biggest performance gains to applications waiting on non-CPU resources e.g. memory
- May not perform well with some applications – real-time applications, time sensitive applications, compute intensive technical applications may perform better with threads off

Multi-Threading
HP-UX 11i v2 and 11i v3 Plans

- **Lead with HP-UX 11i v2 …**
 - Supports early Montecito benchmark results
 - Delivers performance improvements to some applications
 - Exposed to applications/users as virtual CPUs (vCPUs)
 - That can be used or not used on processor set (pset) boundaries
 - On a release shipping in volume
 - But almost certainly with some rough edges
 - Need to characterize how well multi-threading works with typical applications
 - Default will be to ship with multi-threading unused by HP-UX
 - Multi-threading will be turned on in hardware
 - Customer can chose to enable multi-threading within each processor set
 - Some configuration constraints
 - E.g. maximum configuration is 64 x 2 or 128 x 1
- Round out and tune with HP-UX 11i v3 …
 - And, hopefully, ship with multi-threading on by default

Open-VMS & Montecito Technologies

- Multi-threading
 - Yes
- Pellston
 - Yes , not OS dependent
- Foxton
 - Yes
- Silverdale
 - Post announcement HP-VM version

Windows and Montecito Technologies

- Multi-threading
 - Yes , # of supported threads limited in W2003 SP1 64 only
- Pellston
 - Yes , not OS dependent
- Foxton
 - Under-investigation for multiple p-state support
- Silverdale
 - Post announcement HP-VM version

Linux and Montecito Technologies

- Multi-threading
 - Yes
- Pellston
 - Yes , not OS dependent
- Foxton
 - Under-investigation
- Silverdale
 - Post announcement HP-VM version

Summary

- Montecito builds on the capable Itanium® 2 processor and introduces several innovations, and technologies
 - System interface, software, and compatible optimization
 - Performance through traditional frequency, micro-architecture improvements
 - Performance through new technologies such as multiple cores and threads
 - Efficiency to support 2 cores, 2 threads, 26.5MByte of cache, and 1.72 billion transistors at 100W
 - Flexibility in deployment with dynamic power and frequency management and RAS+M that protect data and provide manageability where needed

1.72 Billion transistors at 100W providing the industry with compatibility, performance, efficiency, and flexibility

Thank you!

Ingolf.Buttig@hp.com

Intel new platform component numbers

Today

Itanium 2	MP DP	1.66/9M-667 1.60/9M-400 1.66/6M-667 1.60/6M-400 1.50/4M-400	E8870 Chipset
Xeon	MP	3.33/8M 3 /8M 2.83/4M 3.66/1M 3.16/1M	E8500 Chipset
Xeon	DP	3.60/2M 3.40/2M 3.20/2M 3.00/2M 2.80/2M	E7525 Chipset E7520 Chipset E7320 Chipset
Pentium 4 / Pentium D	UP	Desktop Processor Numbers	E7230 Chipset

2006

Itanium 2	9000	9055 9040/41 9030/31 9020/21 9010/11	Future Chipset TBD
Xeon	7000	7040/41 7030 7020	Future Chipset TBD
Xeon	5000	5070 5060 5050 5040 5030 5020	5000X Chipset 5000P Chipset 5000V Chipset
UP Chipset Only	3000	Desktop Processor Numbers	3000P Chipset

Processor Number



9000

Montecito SKUs

Intel® Itanium® 2 Processor 9040
- **Dual-core / 1.60GHz / 18MB L3 cache / 400/533MHz FSB**
- **Intel® VT, Pellston, Foxton 1.80GHz, HT, DBS**

Intel® Itanium® 2 Processor 9020
- **Dual-core / 1.40GHz / 12MB L3 cache / 400/533MHz FSB**
- **Intel® VT, Pellston, Foxton 1.60GHz, HT, DBS**

Intel® Itanium® 2 Processor 9010
- **1.60GHz / 6MB L3 cache / 400/533MHz FSB**
- **Single-core, Intel® VT, Pellston, Foxton 1.80GHz**

Power Optimized SKU

Intel® Itanium® 2 Processor LV 9018
- **Dual-core / 1.20GHz / 62W / 12MB L3 cache / 400MHz FSB**
- **Intel® VT, Pellston, Foxton 1.40GHz, HT, DBS**

64-bit Intel® Enterprise Processors Feature Set Reference Table

Processor Brand Name	Processor Generation	Process	Processor Number	Clock Speed /TDP GHz (Watt)	Cache	Bus Speed (MHz)	Intel Capabilities						
							HT	64-bit	DBS	Dual Core	VT	Pellston	Foxton (Freq.)
Intel® Itanium® 2 Processor	Montecito	90 nm	9055	1.80	24MB L3	400/533/ 667	√	√	√	√	√	√	2 GHz
			9041	1.60	18MB L3	667	√	√	√	√	√	√	1.80 GHz
			9040	1.60	18MB L3	400/533	√	√	√	√	√	√	1.80 GHz
			9031	1.70	8MB L3	667		√		√	√	√	1.80 GHz
			9030	1.70	8MB L3	400/533		√		√	√	√	1.80 GHz
			9021	1.40	12MB L3	667	√	√	√	√	√	√	1.60 GHz
			9020	1.40	12MB L3	400/533	√	√	√	√	√	√	1.60 GHz
			9011	1.60	6MB L3	667		√			√	√	1.80 GHz
			9010	1.60	6MB L3	400/533		√			√	√	1.80 GHz
	Montecito LV (62W)	90 nm	9018	1.20	12MB L3	400	√	√	√	√	√	√	1.40 GHz
	Madison	.13µ	-	1.66	9MB L3	667		√					
			-	1.60	9MB L3	400		√					
			-	1.66	6MB L3	667		√					
			-	1.60	6MB L3	400		√					
			-	1.50	4MB L3	400		√					
	Fanwood	.13µ	-	1.60	3MB L3	533		√					
			-	1.60	3MB L3	400		√					
	Fanwood LV (62W)	.13µ	-	1.30	3MB L3	400		√					

Intel Enterprise Server Platform Roadmap

Segment/Sockets		2004 -2005	2005-2006	FUTURE
RISC Replacement	4/8+	Intel® Itanium® 2 - 9M cache Intel® E8870 / Enabled	Montecito / Montvale Intel® E8870 / Enabled	Richford / Future Platf Tukwila ('07), Poulson Future chipsets
	2	Intel® Itanium® 2 - 3M cache Intel® E8870 / Enabled	Millington / DP Montvale Intel® E8870 / Enabled	Dimona Future chipset
Enterprise	4/8+	Truland 64-bit Intel® Xeon™ MP – 8M Intel® E8500 / Enabled chipsets	Truland Paxville / Tulsa Intel® E8500 / Enabled	Reidland Whitefield ('07) Future chipset
Volume	2	64-bit Intel® Xeon™ Processor Intel® E7520 and Intel® E7320	Bensley Dempsey Blackford chipset	Future Platform Future Processor Future chipset
Technologies		EPIC Architecture Enhanced MCA Hyper-Threading Technology Intel® EM64T PCI Express* DDR-2 Memory Power Management (DBS)	plus Dual-core Intel® Virtualization Tech Intel® I/O Acceleration Tech FB-DIMM Memory Foxton Technology Pellston Technology Intel® Active Mgmt Tech	plus Multi-core Enhanced Virtualization Enhanced I/O & Memory Enhanced RAS Enhanced Manageability Common Platform Architecture

Dual/Multi-Core

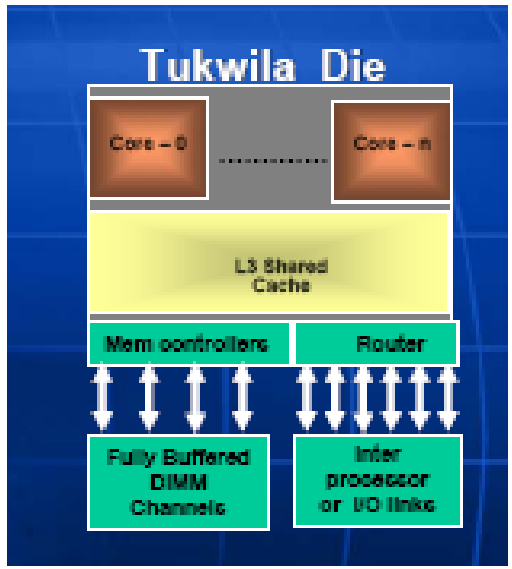
Dates and information are preliminary and subject to change without notice.

Future Itanium® Processor-Tukwila

New micro architecture with point to point interface

Overview/Key Processor Features

- New micro core architecture with multiple cores per die; 65 nm
- Targeting +10 MB L3 shared cache
- Point to point links based interface at 30+ Giga Transfers/sec
- Integrated Fully Buffered DIMM Memory controllers with 25+ GByte bandwidth



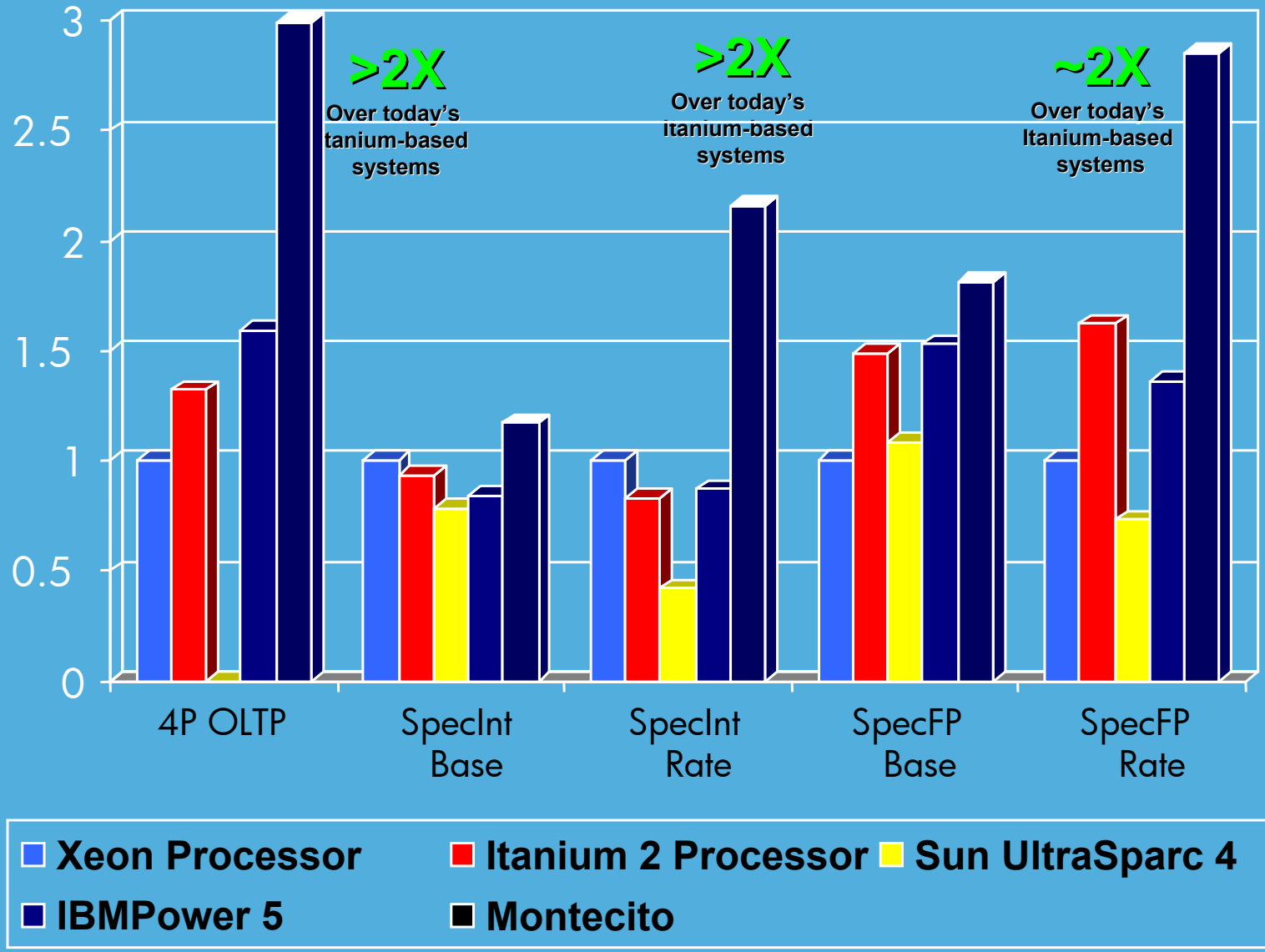
Performance/Power

- Targeting ~4.0 GHz
- Within Madison power/thermal envelope
- Multiple product variants optimized for targeted markets

Platform

- New platform architecture, Fully compatible with Itanium® 2 processor family binaries

Montecito Performance



SPEC CPU2000 numbers on Montecito are estimated numbers and are provided by Intel Corporation based on projections. Actual performance may vary.